Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A method for reading data from a memory to achieve reduced jitter, comprising the steps of:

applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;

applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and

altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity ~~within at least one~~ below a prescribed threshold.

2. (Original) The method according to claim 1 further comprising the step of lengthening the duration of the at least one Read Address to repeat reading of a fractional sample

3. (Original) The method according to claim 2 further comprising the step of lengthening the duration of more than one Read Address to repeat the reading of more than one fractional sample.

4. (Original) The method according to claim 1 further comprising the step of shortening the duration of the at least one Read Address to skip reading of a fractional sample

5. (Original) The method according to claim 4 further comprising the step of shortening the duration of more than one Read Address to skip reading of more than one fractional sample

6. (Original) The method according to claim 1 further comprising the step of applying the successive read clock pulses to the memory at a frequency four times the frequency f_n

7. (Currently amended) A system for reading stored data to achieve reduced jitter, comprising:

a memory into which data is written and from which data is read;

a clock applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data;

a memory address generator for applying successive Read Addresses to the memory at a rate slower than the xf_n frequency of said clock applying successive read clock pulses to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations; and for altering the duration of at least one successive Read Addresses in response to memory usage status to maintain memory capacity ~~within at least one~~ below a prescribed threshold

8. (Original) The apparatus according to claim 7 wherein the memory address generator lengthens the duration of the at least one Read Address to repeat reading of a fractional sample.

9. (Original) The apparatus according to claim 8 wherein the memory address generator lengthens the duration of more than one Read Address to repeat the reading of more than one fractional sample.

10. (Original) The apparatus according to claim 7 wherein the memory address generator shortens the duration of the at least one Read Address to skip reading of a fractional sample

11. (Original) The apparatus according to claim 10 wherein the memory address generator shortens the duration of more than one Read Address to skip reading of more than one fractional sample.

12. (Original) The apparatus according to claim 1 wherein the system clock applies successive read clock pulses to the memory at a frequency four times the frequency f_n